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**EUROPEAN PATENT APPLICATION**

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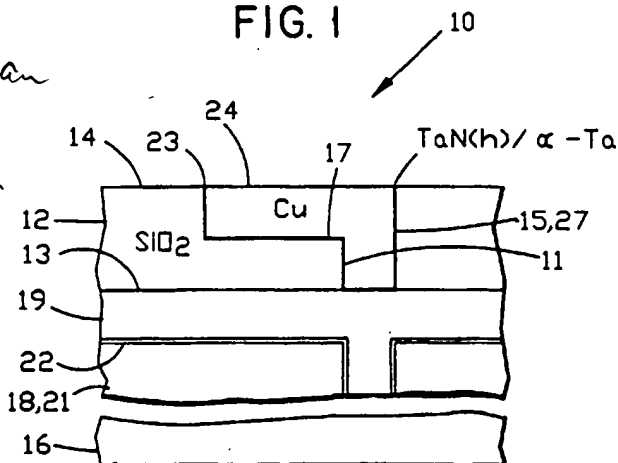
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(57) An interconnect structure and barrier layer for electrical interconnections is described incorporating a layer of TaN in the hexagonal phase between a first material such as Cu and a second material such as Al, W, and PbSn. A multilayer of TaN in the hexagonal

phase and Ta in the alpha phase is also described as a barrier layer. The invention overcomes the problem of Cu diffusion into materials desired to be isolated during temperature anneal at 500°C.

FIG. 1



Combination w/ Colgan  
- reference teachers  
away from combination.  
(col. 2)

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## Description

### Field of the Invention

This invention relates to metal interconnects and more particularly to a metal diffusion barrier and liner for VLSI and ULSI metal interconnects, studs, for CMOS gate stacks on semiconductor chips, and for electrical interconnections in packaging and display devices.

### Background of the Invention

On VLSI and ULSI semiconductor chips, Al and alloys of Al are used for conventional chip wiring material. The incorporation of Cu and alloys of Cu as a chip wiring material results in improved chip performance and superior reliability when compared to Al and alloys of Al. However, Cu must be successfully isolated from the devices formed in the silicon substrate below and from the surrounding back end of the line (BEOL) insulators. To accomplish this isolation i.e. to prevent diffusion of Cu, a thin liner material is deposited on the patterned BEOL insulator e.g. trenches formed in the Damascene process or unpatterned insulator e.g. Cu reactive ion etching (RIE) or through mask Cu deposition process before the Cu is deposited. The thin film liner must also serve as an adhesion layer to adhere the copper to the surrounding dielectric. Adhesion of copper directly to most insulators is generally poor.

TiN has been evaluated as a Cu Barrier and has been reported in the literature as a barrier for Cu interconnects in SiO<sub>2</sub>. in a publication by S-Q Wang MRS Bulletin 19, 30, (1994) entitled "Barriers against copper diffusion into silicon and drift through silicon dioxide", various barrier systems including TiN are shown for placement between Si/SiO<sub>2</sub> and Cu. TiN has good adhesion to SiO<sub>2</sub>. However, Cu adheres poorly to TiN. A very thin glue or adhesion layer of Ti may be used to enhance the adhesion of Cu to TiN; however, this Ti layer drastically degrades the conductivity of the copper film during subsequent thermal processing. In addition, TiN has been known to form corrosion couple with copper in certain copper polishing slurry used in chemical mechanical polishing (CMP).

Unlike TiN, pure or oxygen-doped Ta adheres poorly to some insulators such as SiO<sub>2</sub>. It also forms the high-resistivity beta-phase Ta when deposited directly on the insulator. Furthermore, the Cu barrier properties of Ta fail when it is in contact with Al at moderate temperatures. See for example, the publication by C.-K Hu et al., Proc. VLSI Multilevel Interconn. Conf. 181, (1986) which described an investigation of diffusion barriers to Cu wherein Tantalum, silicon nitride and titanium nitride were found to be the good diffusion barriers to Cu. It is reported that oxygen in the Ta films may have inhibited Cu diffusion.

In a publication by L.A. Clevenger et al., J. Appl. Phys. 73, 300 (1993), the effects of deposition pressure, in situ oxygen dosing at the Cu/Ta interface, hydrogen

and oxygen contamination and microstructure on diffusion barrier failure temperatures for HV and UHV electron-beam deposited Ta thin films penetrated by Cu were investigated.

Ta<sub>2</sub>N has been proposed as a good copper diffusion barrier, but its adhesion to BEOL insulators and copper is relatively poor. In contrast, the adhesion of TaN (N~50%) is adequate, while the adhesion of Cu to TaN is poor. A thin Ta layer can be used to enhance the adhesion of Cu to TaN, without the Ta degrading the performance of Cu BEOL. Such a dual-component liner has been previously disclosed in U.S. patent 5,281,485 Jan. 25, 1994 to E.G. Colgan and P.M. Fryer. However, the resistivity of this TaN is at least 1200 Micro Ohm-cm, which leads to larger vias or stud resistances, and the inability of the metal liner to act as a redundant current strap or path.

For deep-submicron vias (e.g. less than 0.5 um wide) with ~250 A liner at the bottom, the series resistance of the above Ta-based liners is in the range from 1 to 5 Ohms. By contrast, the copper stud resistance would be less than 10% of the Ta based liner. Although these via resistances compare very favorably with those of Al(Cu)/W-stud values, it is desirable to reduce them below the 1 Ohm range.

### Summary of the Invention

In accordance with the present invention, a barrier layer is provided comprising a layer of TaN in the hexagonal phase positioned between a first material to be confined and a second material whereby the second material is isolated from said first material. The first material may be one or a combination of Cu, Al, W and PbSn.

The invention further provides a layer of TaN in the hexagonal phase may be positioned between the gas WF6 and a second material to be isolated from the first material.

The invention further provides an interconnect structure comprising a first insulation layer having an upper and lower surface and having a plurality of grooves formed in the upper surface, some of the grooves having regions extending to the lower surface to expose respective conducting surfaces in a second interconnect structure below the first insulation layer, a liner including a layer of TaN in the hexagonal phase formed on the sidewalls and bottom of the plurality of grooves and on the exposed respective conducting surfaces, and a metal formed in the plurality of grooves to substantially fill the plurality of grooves.

The invention further provides a liner or barrier layer for VLSI/ULSI interconnects and C4 solder bumps made mostly of Pb-Sn which simultaneously achieves good diffusion barrier performance, good adhesion to BEOL insulators, good adhesion of interconnect metal to this liner, low resistivity, and good conformality in trenches and vias. The interconnects and studs may comprise aluminum, copper, tungsten, or C4 solder balls

made of lead-tin alloy.

The invention provides a liner composed of predominately highly oriented and non-highly oriented (random) hexagonal phase TaN (30-60% nitrogen) (which may contain up to 50% cubic phase TaN) deposited alone or as a thin film laminate in combination with other suitable metal films such as Ta. Preferably, the TaN is 100% hexagonal phase.

The liner material described above provides a high integrity barrier, low stress, low resistivity and excellent adhesion to both metal and various dielectrics, such as polymers, silicon dioxide, BPSG, and diamond-like carbon and isolates lead-tin solder metallurgy from Cu and Al interconnects.

The invention further provides a thin film material for isolating Al wiring levels from an immediate Cu interconnection level above or below.

The invention further provides a liner which isolates a metal layer of W, Cu, alloys of Cu, Al and alloys of Al from the contact silicide ( $\text{WSi}_2$ ,  $\text{CoSi}_2$ ,  $\text{TiSi}_2$ ,  $\text{TaSi}_2$  and  $\text{PtSi}$ ) and polycrystalline silicon in a MOSFET (metal oxide semiconductor field effect transistor) gate stack.

The invention further provides a liner to shield existing metal from certain gases such as  $\text{WF}_6$  which is corrosive used as a precursor gas for the deposition of W.

The invention further provides a liner which provides good contact resistance to preceding levels of metal, such as aluminum in BEOL wiring.

The invention further provides a liner which provides markedly better conformality than Ti-based compounds even without collimation sputtering or chemical vapor deposition (CVD).

The invention further provides a thin film to isolate BEOL interconnect metals from alloying or mixing with the lead-tin in for example, C4 solder balls.

The invention further provides a liner material exhibiting good conformality when deposited in trenches and vias BEOL structures.

The invention further provides a liner material which will not form a corrosion couple with Cu, Al, or W during or after chemical mechanical polishing of the liner material.

#### Brief Description of the Drawing

These and other features, objects, and advantages of the present invention will become apparent upon consideration of the following detailed description of the invention when read in conjunction with the drawing in which:

Fig. 1 is a cross section view of one embodiment of the invention.

Fig. 2 is a cross section view of a second embodiment of the invention.

Fig. 3 is a cross section view of a third embodiment of the invention.

Fig. 4 is a cross section view of a fourth embodiment of the invention.

Fig. 5 is a graph of an X-ray diffraction pattern for a

TaN (hexagonal) film.

Fig. 6 is a Transmission Electron Microscope (TEM) micrograph of a diffraction pattern from TaN (hexagonal) film.

Fig. 7A is a Transmission Electron Microscope (TEM) micrograph of the same highly oriented TaN (hexagonal) film used to provide the X-ray diffraction pattern of Fig 5.

Fig. 7B is a Transmission Electron Microscope (TEM) micrograph of non-highly oriented (random) TaN (hexagonal) film.

Fig. 8 is a graph of the resistance versus temperature profile of a  $\text{SiO}_2/\text{Cu}/\text{TaN}$  (hexagonal)/Al layered structure.

Fig. 9 is a cross-section view of a liner of TaN (hexagonal) for isolating Cu from Al.

Fig. 10 is a cross section view of a fifth embodiment of the invention.

#### Description of the Preferred Embodiment

Referring to the drawing and more particularly to Fig. 1, a cross section view of interconnect structures 10 and 18. Interconnect structure 10 includes a layer of insulation 12 having an lower surface 13 and an upper surface 14. A plurality of grooves or trenches 15 are formed in upper surface 14 of insulation layer 12. The plurality of grooves 15 may correspond to a wiring layer of a semiconductor chip 16. Additional interconnect structures may be provided to complete the interconnections for a semiconductor chip 16. Vias or stud openings 11 are formed at the bottom 17 of grooves 15 in selected regions to make contact to conducting surfaces in a second interconnect structure 18 below the insulation layer 12.

Interconnect structure 18 has a conductor 19 in a groove 20 in insulation layer 21. A liner 22 is shown between conductor 19 and the bottom and sidewalls of groove 20.

A liner 23 of TaN (hexagonal) is formed in grooves 15 on the sidewalls 27 and bottom 17 followed by formation of metal 24 in grooves 15 to substantially fill grooves 15. Metal 24 may be Cu, Al, W and alloys thereof. Metal 24 may be formed by sputtering, physical vapor deposition (PVD), chemical vapor deposition (CVD) or electroplating. Liner 23 may be formed by sputtering in an atmosphere of nitrogen. Liner 23 may include a second layer of Ta (alpha phase) formed adjacent to such as over TaN (hexagonal).

Insulation layer 12 as well as insulation layer 21 may be for example  $\text{SiO}_2$ ,  $\text{Si}_3\text{N}_4$ , polymer such as polyamide, diamond-like carbon (DLC) and Fluorinated diamond-like carbon (F-DLC).

Where liner 23 is a highly oriented layer of TaN in the hexagonal phase, the resistivity will be in the range from 150 to 300 micro ohm-cm. Where liner 23 is a non-highly oriented layer of TaN in the hexagonal phase, the resistivity will be greater than 300 micro ohm-cm. Where a layer of Ta in the alpha phase is formed adja-

cent the TaN (hexagonal), the resistivity of the Ta (alpha phase) will be in the range from 15 to 60 micro ohm-cm.

Fig. 2 is a cross section view of interconnect structure 34. Fig. 2 shows a semiconductor substrate 16 which may be for example Si, SiGe, Ge, or GaAs. Above substrate 16 may be a layer of insulation 35 which may be for example silicon dioxide. A layer of insulation 36 may be formed over layer of insulation 35 having a groove or trench 38 formed therein filled with metal 24. Layer of insulation 36 and metal 24 may be a coplanar upper surface 39 formed by chemical-mechanical polishing (CMP). Layer of insulation 40 is formed on upper surface 39. A groove or trench 42 is formed in layer of insulation 40 down to metal 24. A liner 23 is formed on the sidewalls and bottom of groove 42 and on the upper surface 43 of layer of insulation 40 (not shown). Groove or trench 42 is filled with metal 46 over liner 23 and on the liner on upper surface 43 (not shown). The excess metal 46 and liner 23 are removed by CMP to provide a planarized upper surface 43 as shown in Fig. 2. In Fig. 2, metal 24 may be for example Al and metal 46 may be tungsten.

Fig. 3 is a cross section view of interconnect structure 50. In Fig. 3, semiconductor substrate 16 has an insulation layer 52 thereover which may be formed by thermal oxidation. A layer 54 of insulation is formed on upper surface 53 on insulation layer 52. A groove or trench 56 is formed in insulation layer 54 and filled with metal 24 and may be for example Al. Insulation layer 54 and metal 24 may have a coplanar upper surface 58 formed by CMP. A layer 12 of insulation is formed on upper surface 58. Layer 12 has an upper surface 14. A groove 15 and via 11 is formed in upper surface 14. A liner 23 is formed on sidewalls 27 and bottom 17 of groove 15 and via 11. Metal 24 is formed over liner 23 in groove 15 and via 11. Upper surface 14 is planar which may be formed by CMP. A layer of insulation 62 is formed on upper surface 14. An opening 64 is formed in layer 62 to expose metal 24'. Liner 23' is formed on the sidewalls 65 of opening 64 and on exposed metal 24. A blanket metal layer 66 is formed on upper surface 67 on insulation layer 62 and metal 24'. Blanket metal layer 66 is etched through a mask not shown to form a metal pattern for wiring or interconnects. In Fig. 3, metal layer 66 may be for example Al. Metal 24' may be for example Cu and metal 24 may be for example Al.

Thus as shown in Fig. 3, liner 23 separates metal 24 and 24' and liner 23' separates metal 24' and metal 66.

Fig. 4 is a cross section view of interconnect structure 70. In Fig. 4, substrate 16 has a layer of insulation 72 thereover which may be for example silicon dioxide. Interconnect structure 12 is formed over layer of insulation 72.

Insulation layer 62 is formed on upper surface 14. An opening 64 is formed in layer 62 to expose metal 24'. Liner 23' is formed on the sidewalls 65 of opening 64 and on exposed metal 24. A C4 contact bump 74 of

mostly Pb-Sn is formed on liner 23' in opening 64. The C4 bump is manufactured by the IBM Corp on integrated circuit chips for making interconnections. The C4 bump extends above the integrated circuit chip by about 0.125 millimeters and is round or circular in cross-section parallel to the plane of the upper surface of the integrated circuit chip and is curved from its sides to the top surface of the bump where an interconnection is made to another electrode supported by a substrate.

In Figs. 2-4, like references are used for functions corresponding to the apparatus of Fig. 1 or of an earlier Fig. than the Fig. being described.

Fig. 5 is a graph of an X-ray diffraction pattern for a TaN (hexagonal phase) film formed by physical vapor deposition (PVD). The following PVD arrangement was used to provide highly-oriented and non-oriented TaN (hexagonal) films. The TaN (hexagonal) films were reactively sputter deposited using a magnetron system in either the direct current or radio frequency mode i.e. dc or rf mode. The highly oriented and non-oriented TaN (hexagonal) films made under the above conditions had resistivities in the range from 150 to 800 micro ohm-cm. In Fig. 5, the ordinate represents intensity and the abscissa represents two theta. Curve 76 shows the X-ray diffraction pattern for two films; the first film has a high degree of preferred orientation and the second film is a non-oriented film. Curve portion 78 shows a single peak at about 37 degrees.

Fig. 6 is a Transmission Electron Microscope (TEM) diffraction pattern of a TaN (hexagonal phase) highly oriented film previously measured with X-rays in Fig. 5. The micrograph confirms the hexagonal structure of the TaN barrier showing rings indexed to the hexagonal phase.

Fig. 7A is a Transmission Electron Microscope (TEM) micrograph of a TaN (hexagonal phase) film previously measured with X-rays in Fig. 5. The micrograph shows hexagonal TaN grains which are highly oriented and approximately 20-30 nm in size.

Fig. 7B is a Transmission Electron Microscope (TEM) micrograph of a TaN (hexagonal phase). The micrograph shows hexagonal TaN grains which are randomly oriented and also approximately 20-30 nm in size.

Fig. 8 is a graph of the resistance versus temperature provided of a SiO<sub>2</sub>/Cu/TaN (hexagonal)/Al multi-layer structure. In Fig. 8, the ordinate represents resistance in ohms/square and the abscissa represents Temperature in degrees Centigrade. Curve 80 shows the resistance with increasing temperature and curve 82 shows the resistance with decreasing temperature. Curves 80 and 82 provide evidence of the effectiveness of TaN (hexagonal) in isolating Cu from Al up to temperatures greater than 500 degrees Centigrade.

Fig. 9 is a cross-section view of a liner of TaN (hexagonal) to isolate Cu from Al. In Fig. 9, an interconnect structure is shown with a layer of Al(Cu) 84, insulation layer 85 of SiO<sub>2</sub>, and opening or via 86 with a liner 87 on the bottom and sidewalls. Opening 86 is filled with Cu

88 inside liner 87. The excess liner 87 and Cu 88 is removed to form upper surface 89 on insulation layer 85 and upper surface 90 of Cu 88 by CMP. After a temperature anneal at 500 degrees Centigrade for 6 hours, the integrity and the definition of liner 87 remains showing no penetration of Cu through liner 87 to the Al(Cu) layer.

Fig. 10 is a cross-section view which depicts the disclosed TaN(hexagonal) barrier used between the silicide gate contact and the W stud in a P-MOSFET (P-type metal oxide semiconductor field effect transistor).

TaN has the advantage as published that it acts to seed only the low-resistivity alpha phase Ta ( $\rho = 15$  to 60 micro ohm-cm), in contrast to the higher-resistivity beta phase Ta. By using TaN (hexagonal), the resulting via resistances for deep-submicron copper vias with a composite TaN (hexagonal)/ alpha phase Ta liner would be in the resistivity range from 0.25 to 1 Ohms. This resistivity is a substantial improvement, about 5 times better, over the previous copper via systems using Ta alone or another material. The resistivity is probably an order of magnitude better than the Al(Cu)/W via system presently used by some major semiconductor manufacturers.

While there has been described and illustrated a barrier layer and an interconnect structure containing a layer of TaN (hexagonal phase) alone or with a second layer of Ta (alpha phase), it will be apparent to those skilled in the art that modifications and variations are possible without deviating from the broad scope of the invention which shall be limited solely by the scope of the claims appended hereto.

#### Claims

1. A barrier layer comprising:
  - a layer of TaN (23) in the hexagonal phase positioned between a first material (24) to be confined and a second material (12) whereby said second material is isolated from said first material.
2. The barrier layer of claim 1 wherein said first material is selected from the group consisting of Cu, alloys of Cu, Al, alloys of Al, W, and PbSn.
3. The barrier layer of claim 1 wherein said second material is selected from the group consisting of SiO<sub>2</sub>, spin-on-glass, Si<sub>3</sub>N<sub>4</sub>, polyamide, diamond-like carbon (DLC), and fluorinated diamond-like carbon (F-DLC), WSi<sub>2</sub>, CoSi<sub>2</sub>, TiSi<sub>2</sub>, PtSi.
4. The barrier of claim 1 wherein said layer of TaN in the hexagonal phase is highly oriented having a resistivity in the range from 150 to 300 micro ohm-cm.
5. The barrier of claim 1 wherein said layer of TaN in the hexagonal phase is non-highly oriented having a resistivity greater than 300 micro ohm-cm.
6. The barrier layer of claim 1 further including a Ta layer formed adjacent to said layer of TaN.
7. The barrier layer of claim 6 wherein said Ta layer is in the alpha phase.
8. The barrier layer of claim 7 wherein said Ta layer is formed on said layer of TaN.
9. The barrier layer of claim 8 wherein said Ta layer has a resistivity in the range from 15 to 60 micro ohm-cm.
10. An interconnect structure comprising:
  - a first insulation layer having an upper and lower surface and having a plurality of grooves formed in said upper surface, some of said grooves having regions extending to said lower surface to expose respective conducting surfaces in a second interconnect structure below said first insulation layer,
  - a liner including a layer of TaN hexagonal phase formed on the sidewalls and bottom of said plurality of grooves and on said exposed respective conducting surfaces; and
  - a metal formed in said plurality of grooves to substantially fill said plurality of grooves.
11. The interconnect structure of claim 10 wherein said metal is selected from the group consisting of Cu, Al, and W and alloys thereof.
12. The interconnect structure of claim 10 wherein said first insulation layer includes a material selected from the group consisting of SiO<sub>2</sub>, spin-on-glass, Si<sub>3</sub>N<sub>4</sub>, polyamide, diamond-like carbon (DLC) and fluorinated diamond-like carbon (F-DLC).
13. The interconnect structure of claim 10 wherein said layer of TaN in the hexagonal phase is highly oriented having a resistivity in the range from 150 to 300 micro ohm-cm.
14. The interconnect structure of claim 10 wherein said layer of TaN in the hexagonal phase is non-highly oriented having a resistivity greater than 300 micro ohm-cm.
15. The interconnect structure of claim 10 wherein said liner further includes a layer of Ta adjacent said TaN in the hexagonal phase.
16. The interconnect structure of claim 12 wherein said Ta layer is in the alpha phase.

17. The interconnect structure of claim 14 wherein said Ta layer has a resistivity in the range from 15 to 60 micro ohm-cm.
18. The interconnect structure of claim 10 wherein said interconnect structure is formed on a semiconductor chip. 5
19. The interconnect structure of claim 10 wherein said interconnect structure is formed on a display device. 10
20. A gate stack over a channel of a MOS transistor comprising:
- a layer SiO<sub>2</sub>,  
a layer of poly crystalline silicon,  
a layer of TaN (hexagonal); and  
a metal layer whereby atoms of said metal layer are isolated from said polycrystalline silicon layer. 15 20
21. The gate stack of claim 20 wherein said metal is selected from the group consisting of W, Cu, alloys of Cu, Al, and alloys of Al. 25
22. The gate stack over a channel of a MOS transistor comprising:
- a layer of SiO<sub>2</sub>,  
a layer of poly crystalline silicon,  
a layer of silicide,  
a layer of TaN (hexagonal); and  
a metal layer whereby atoms of said metal layer are isolated from said silicide layer. 30 35
23. The gate stack of claim 21 wherein said layer of a silicide is a silicide selected from the group consisting of WSi<sub>2</sub>, CoSi<sub>2</sub>, TiSi<sub>2</sub>, TaSi<sub>2</sub> and PtSi. 40
24. The gate stack of claim 22 wherein said metal is selected from the group consisting of W, Cu, alloys of Cu, Al, and alloys of Cu. 45 50 55

FIG. 1

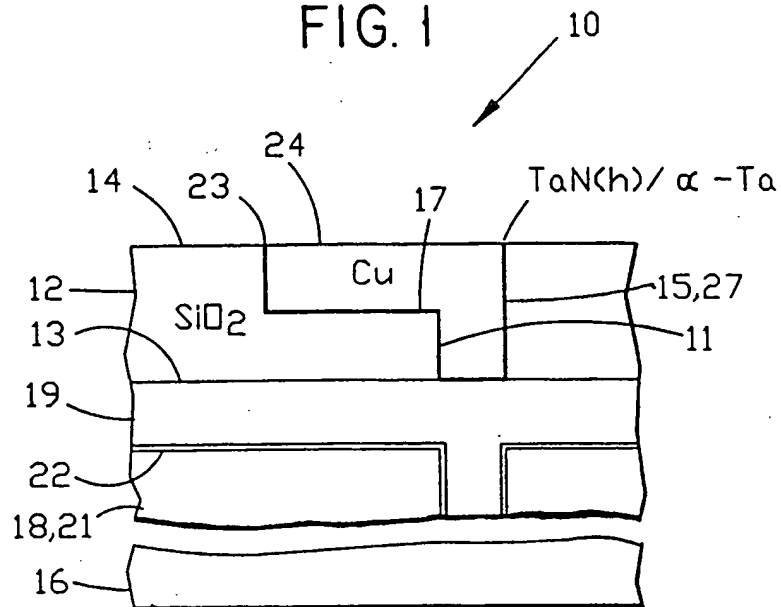


FIG. 2

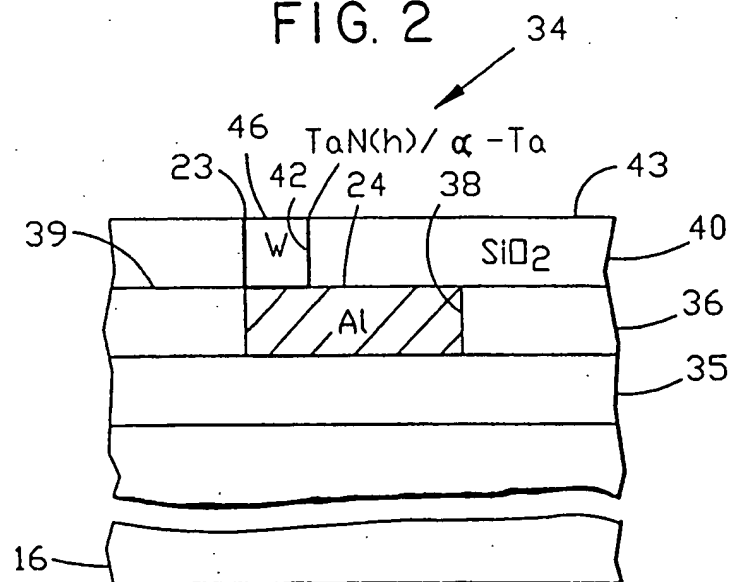


FIG. 3

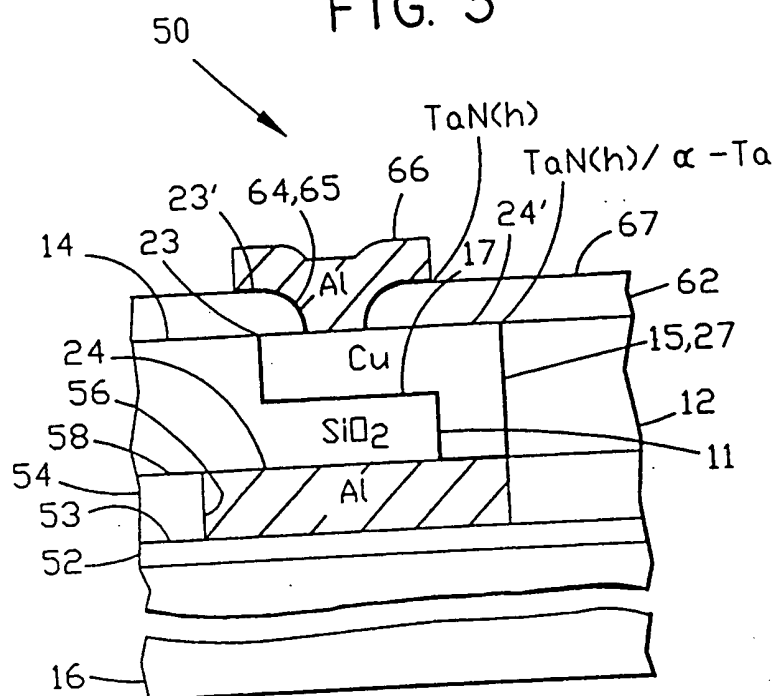
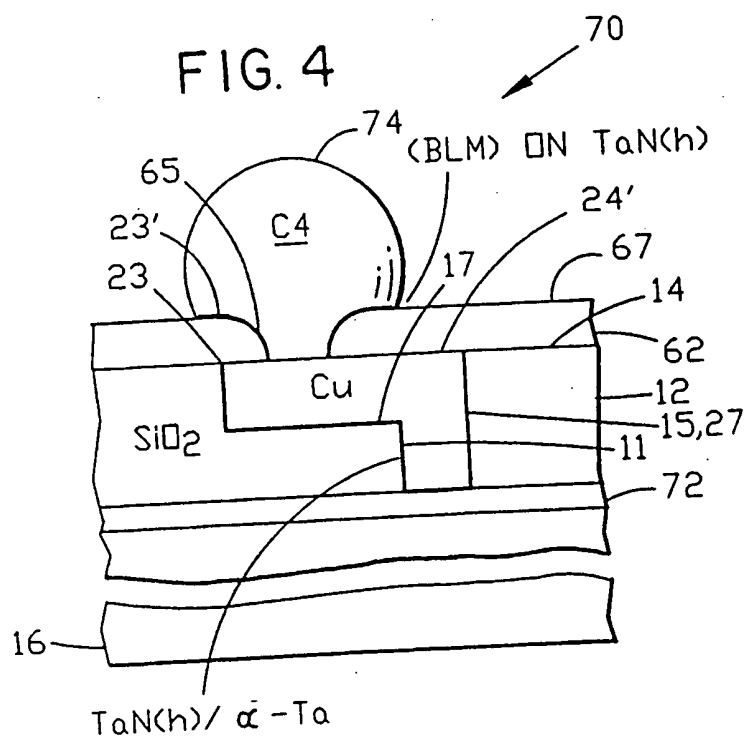
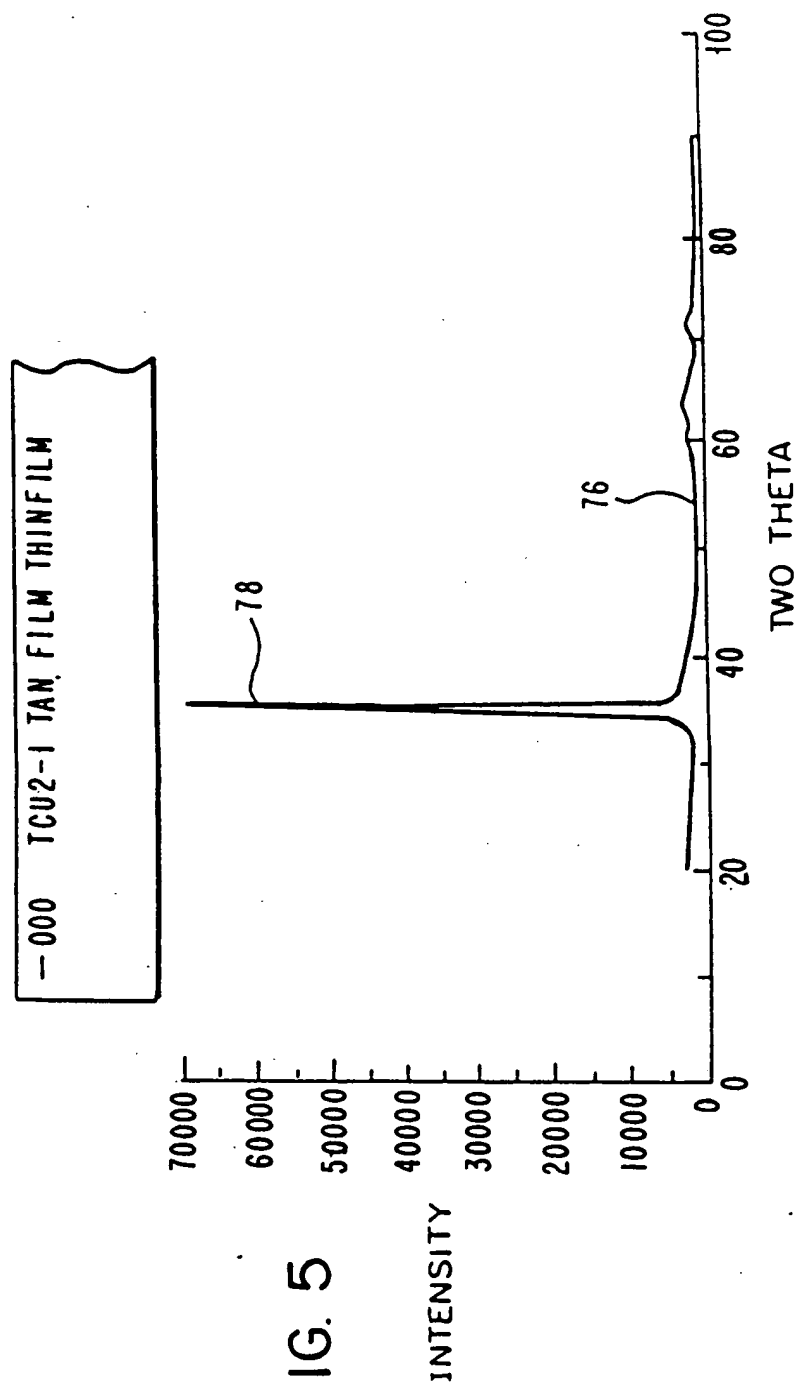


FIG. 4







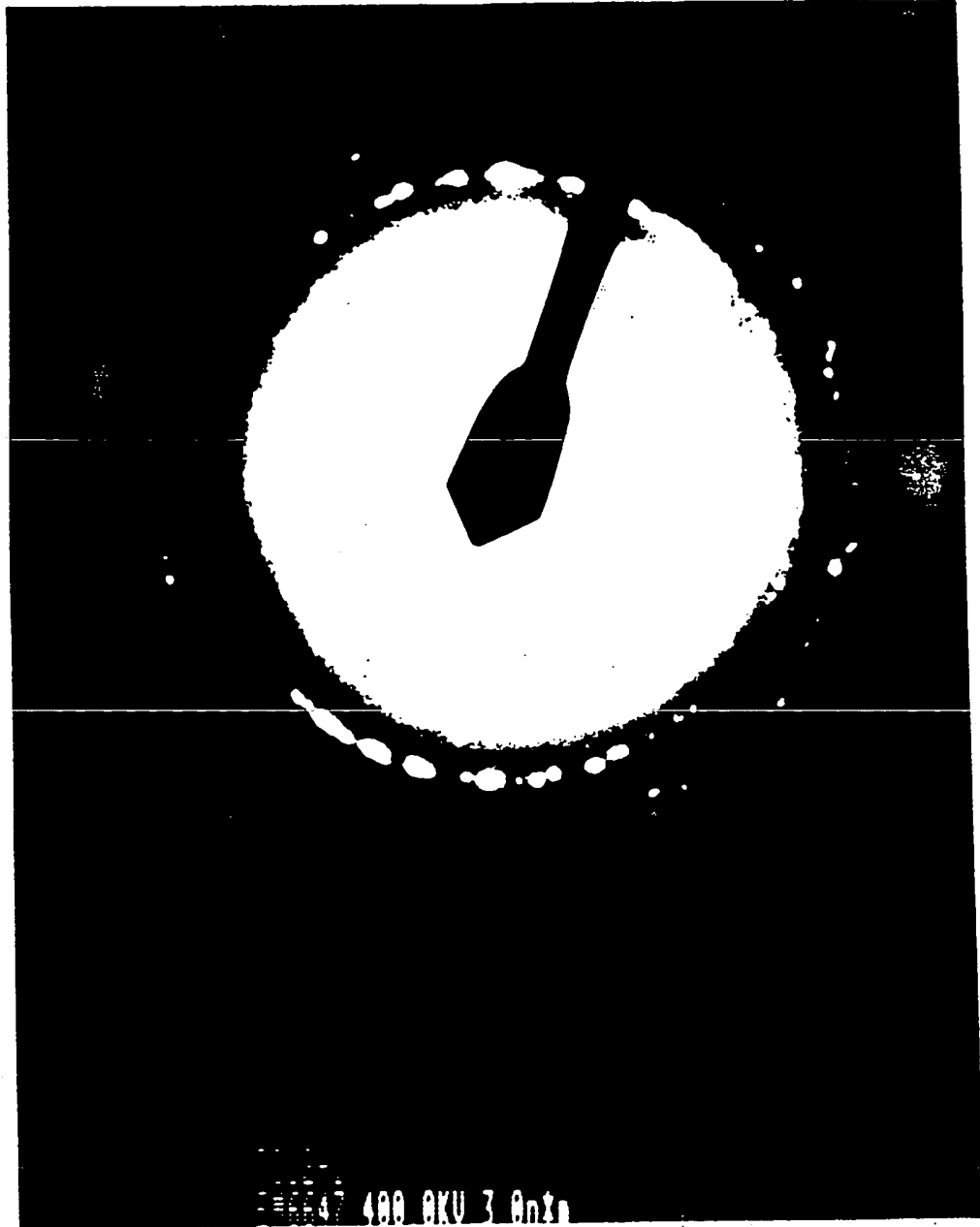


FIG. 6

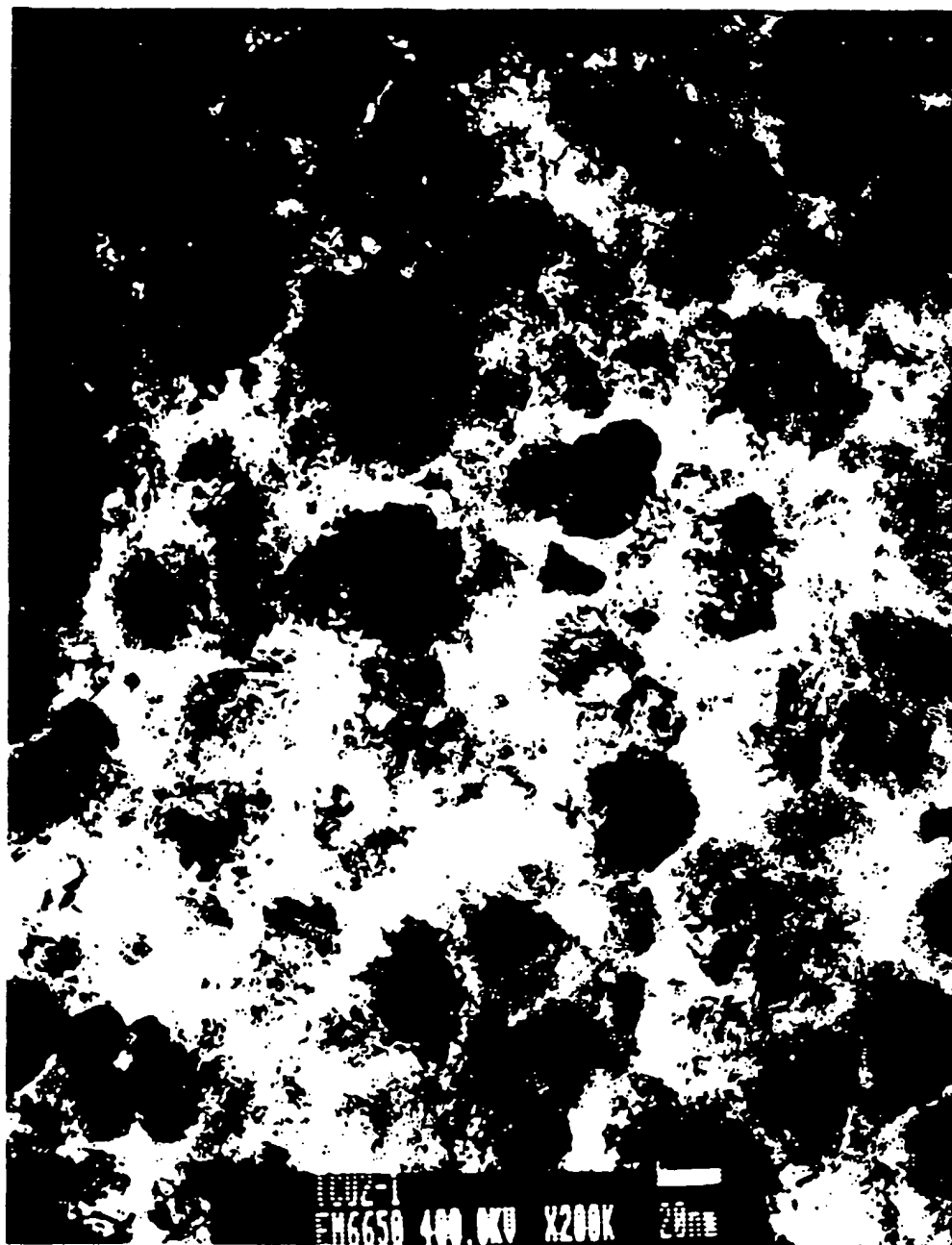


FIG.7A

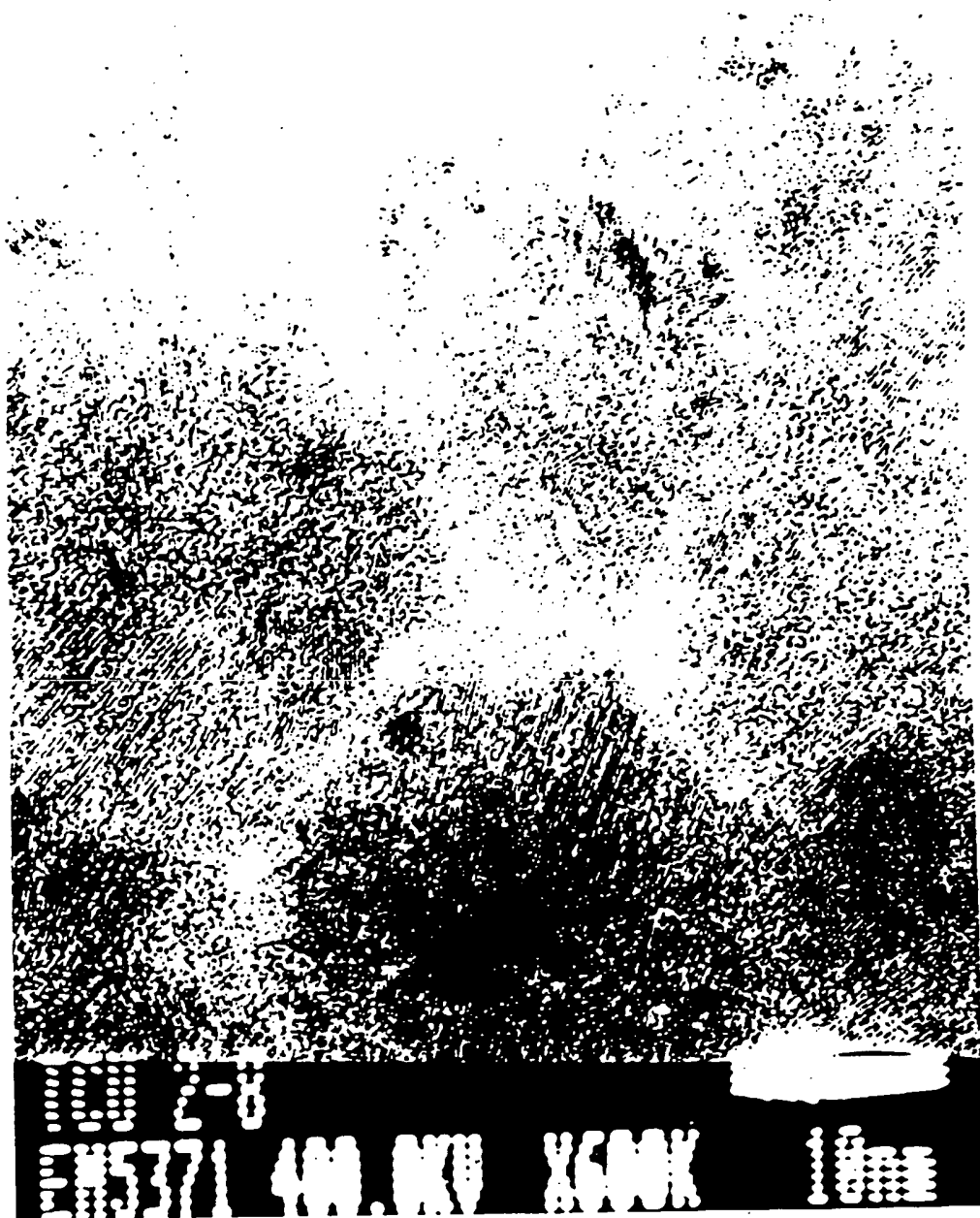


FIG. 7B

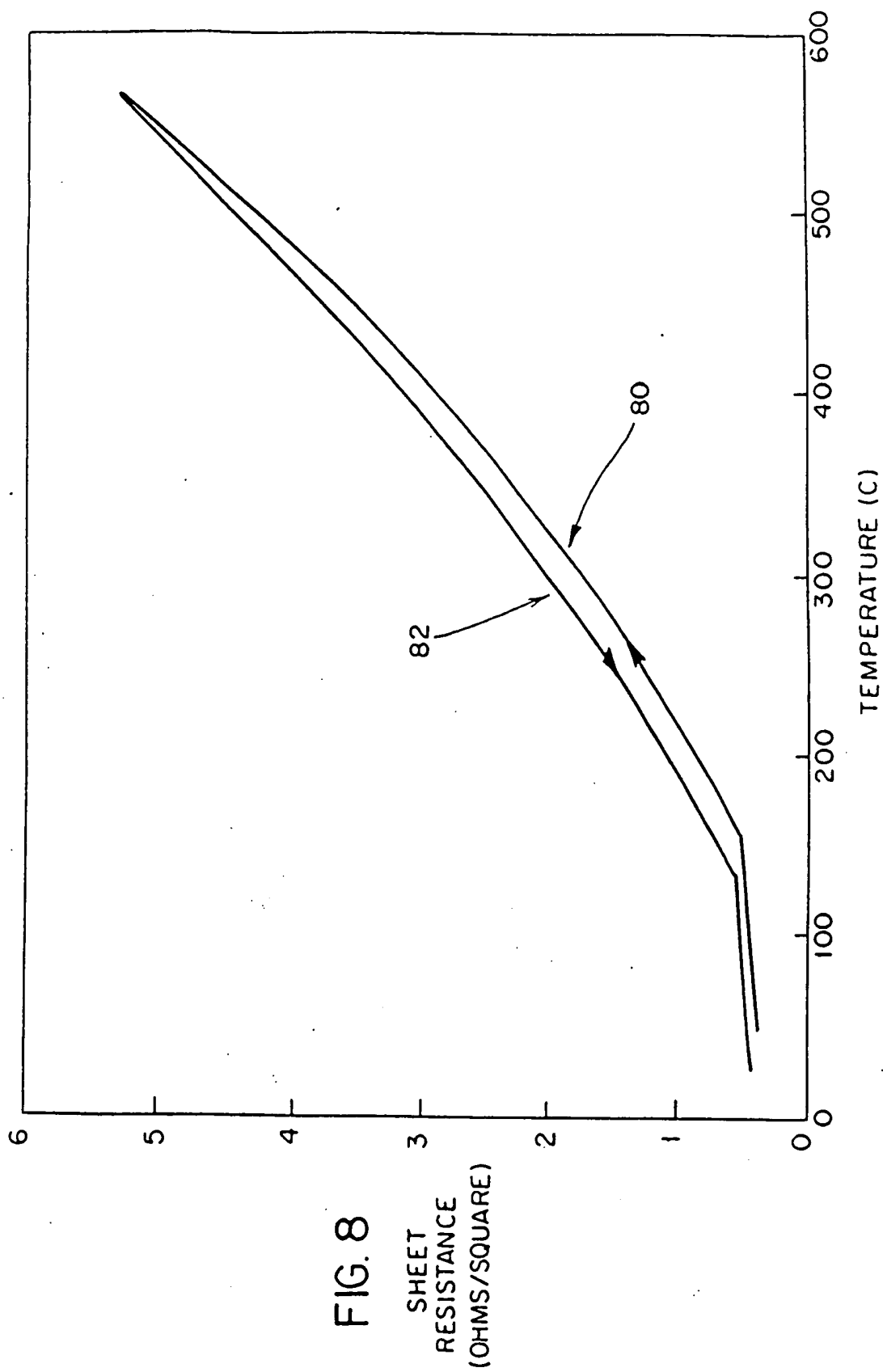


FIG. 8

SHEET  
RESISTANCE  
(OHMS/SQUARE)

TEMPERATURE (C)

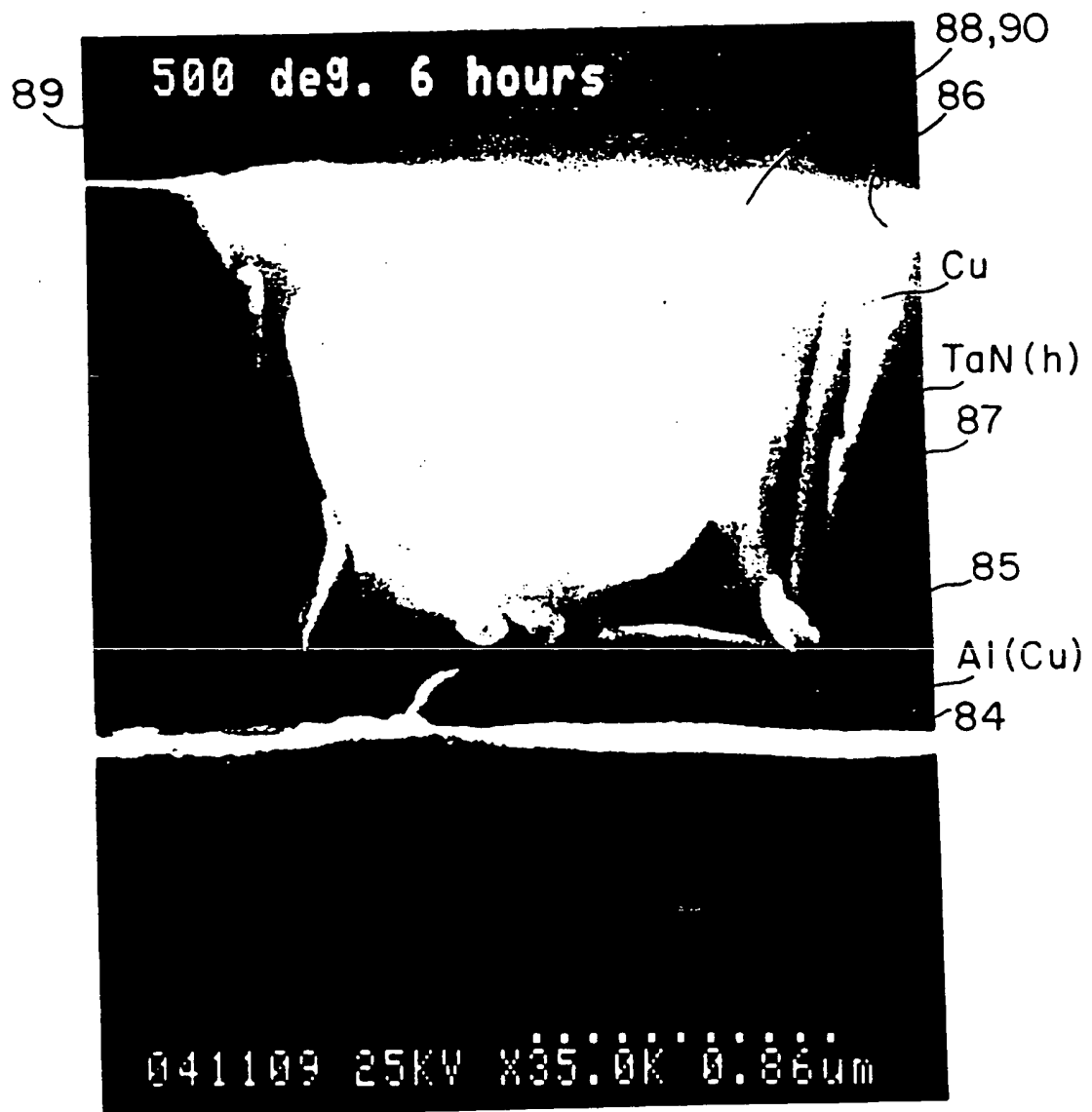
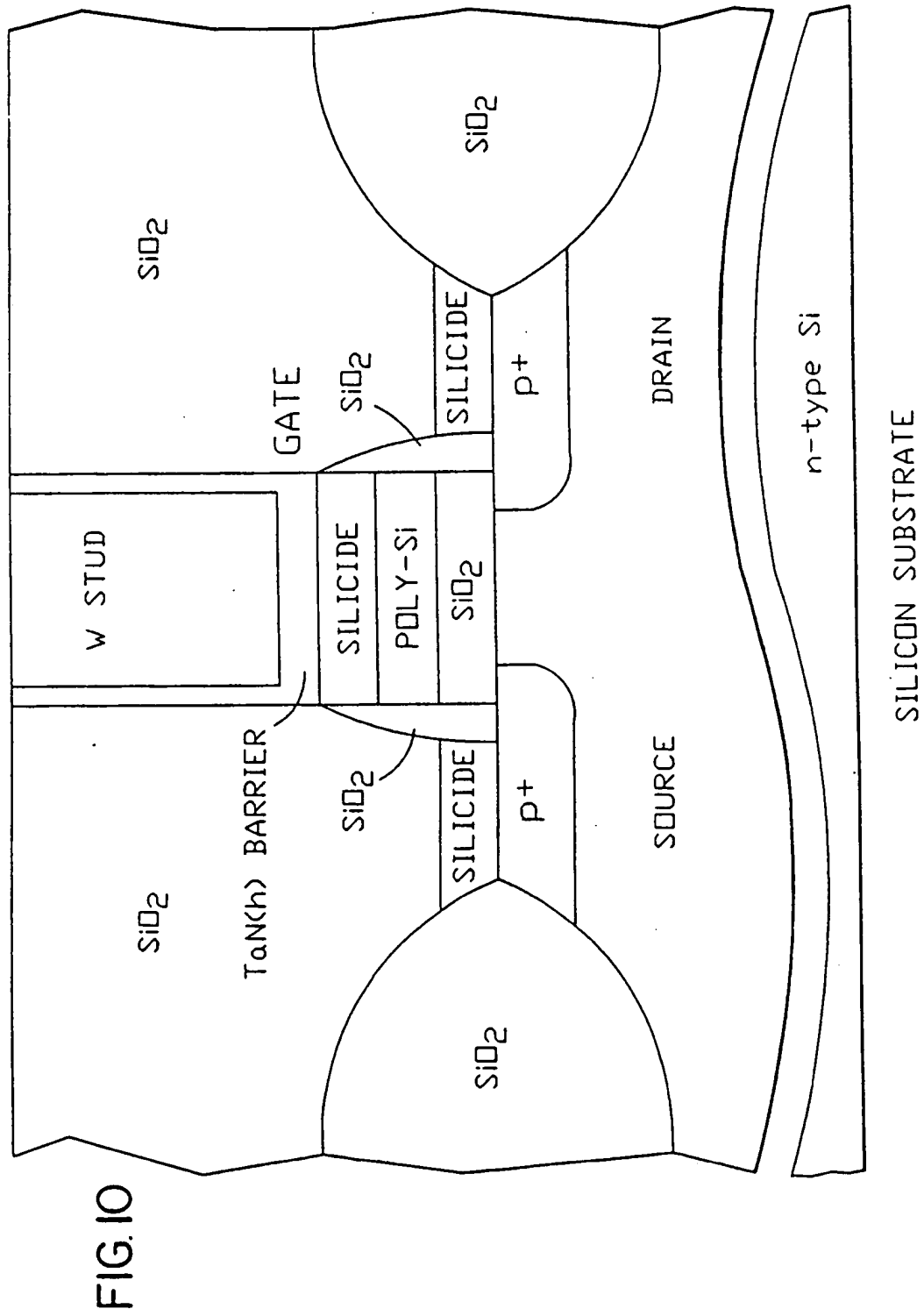
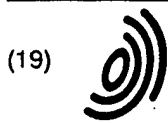


FIG. 9



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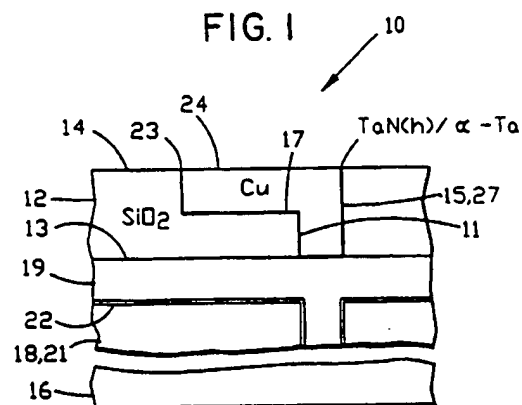
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### (54) A thin film metal barrier for electrical interconnections

(57) An interconnect structure (10) and barrier layer for electrical interconnections is described incorporating a layer of TaN (23) in the hexagonal phase between a first material such as Cu and a second material such as Al, W, and PbSn. A multilayer of TaN in the hexagonal phase and Ta in the alpha phase is also described as a barrier layer. The invention overcomes the problem of Cu diffusion into materials desired to be isolated during temperature anneal at 500°C.



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European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 96 10 9354

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
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A	* page 5433, right-hand column, paragraph 3 - page 5435, left-hand column, paragraph 1 *	10,11, 20-22,24	
A	* page 5439, left-hand column, paragraph 1 - page 5440, right-hand column, paragraph 1 *		
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A	IBM TECHNICAL DISCLOSURE BULLETIN, vol. 23, no. 7b, December 1980, pages 3227-3228, XP002019321 J.K. HOWARD ET AL: "Improved process for gold metallisation" * the whole document *	1,2,4,5, 10,13, 14,18, 20,22	
The present search report has been drawn up for all claims			
Place of search BERLIN		Date of completion of the search 25 November 1996	Examiner Le Minh, I
<p><b>CATEGORY OF CITED DOCUMENTS</b></p> <p>X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document</p> <p>T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons A: member of the same patent family, corresponding document</p>			

EPO FORM 150 (01.92) (P0401)



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 96 10 9354

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	EP-A-0 024 863 (FUJITSU LTD) 11 March 1981  * page 4, line 36 - page 5, line 32; figure 1 *	1,4-10, 13-17, 20,22	
A	--- EP-A-0 568 108 (FAIRCHILD SEMICONDUCTOR) 3 November 1993  * column 3, line 33 - column 6, line 22; figure 3 *	1,5-10, 14-17, 20,22,23	
D,A	--- WO-A-92 07968 (IBM) 14 May 1992  * page 9, line 9 - page 11, line 22; figures 2A,3A *	1,6-10, 15-17, 20,22	
			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
The present search report has been drawn up for all claims			
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